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NO. 817 P. 1

## **BEYER WEAVER & THOMAS, LLP**

**INTELLECTUAL PROPERTY LAW**

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### **FACSIMILE COVER SHEET**

October 4, 2004

**Receiver: Office of Initial Patent Examination  
Filing Receipt Corrections**

**TEL #:**

**FAX # : 703-746-9195**

**Sender: Francis T. Kalinski II, Esq.**

**Our Ref. No.: 02-0279/1D / LSIIP199D1**

**Re: App. No. 10/623,082  
Filing Date: July 17, 2003**

**Pages Including Cover Sheet(s): 4**

**MESSAGE:**

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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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In re application of: BURKE et al.

Attorney Docket No.:  
02-0279/1D / LSI1P199D1

Application No.: 10/623,082

Examiner: BROCK II, Paul E.

Filed: July 17, 2003

Group: 2815

Title: INTER-LAYER INTERCONNECTION  
STRUCTURE FOR LARGE ELECTRICAL  
CONNECTIONS

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**CERTIFICATE OF FACSIMILE TRANSMISSION**

I hereby certify that this correspondence is being transmitted by facsimile to fax number 703-746-9195 to the Office of Initial Patent Examination's Filing Receipt Corrections, on October 4, 2004.

Signed: 

Sue Funchess

**REQUEST FOR CORRECTED FILING RECEIPT**Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

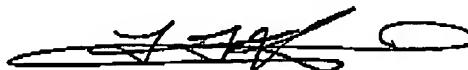
Sir:

Attached is a copy of the Filing Receipt for the above-identified patent application.  
Please reprint the Filing Receipt as follows and mail the corrected copy to the undersigned.

Change the Applicant's name "Pete A. Burke" to -- Peter A. Burke --.

Change the "Small Entity" status to -- Large Entity -- status.

Since this is a Patent Office typographical error, no fee should be due. However, the Commissioner is authorized to charge any fees that may be due to Deposit Account 12-2252 (Order No. 02-0279/1D).

Respectfully submitted,  
BEYER WEAVER & THOMAS, LLPFrancis T. Kalinski II  
Registration No. 44,177P.O. Box 778  
Berkeley, CA 94704-0778



## UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/623,082	07/17/2003	2811	375	02-0279/1D / LSI1P199D1	5	7	1

CONFIRMATION NO. 3302

24319  
LSI LOGIC CORPORATION  
1621 BARBER LANE  
MS: D-106 LEGAL  
MILPITAS, CA 95035

## FILING RECEIPT



\*OC000000011069291\*

OCT 2 4 2003

Date Mailed: 10/21/2003

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

*Peter*  
Pete A. Burke, Portland, OR;  
William K. Barth, Gresham, OR;

## Assignment For Published Patent Application

LSI Logic Corporation;

## Domestic Priority data as claimed by applicant

This application is a DIV of 10/272,767 10/16/2002 PAT 6,642,597

## Foreign Applications

If Required, Foreign Filing License Granted: 10/20/2003

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No

\*\* SMALL ENTITY \*\*

Title

*Large Entity*

Inter-layer interconnection structure for large electrical connections

Preliminary Class

257

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